IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER (Large Entity)

Application Number: **09/966,095**

Group Art Unit: **2111**

Filed: **October 1, 2001**

Examiner Name: **Dang, Khanh**

Applicant: **Balay et al.**

Attorney Docket Number: **Balay 2-1**

TITLE: **PCI/LVDS HALF BRIDGE**

Total Number of Pages in this Submission: **19**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

Transmitted herewith is:
(Corrected) Appeal Brief – 18 pages.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED					
	CLAIMS REMAINING AFTER Amendment	HIGHEST # PREV. PAID FOR	# OF EXTRA CLAIMS	RATE	ADDITIONAL FEE
Total Claims	21	26	0	x $18 =	$ 0.00
Independent Claims	3	3	0	x $86 =	$ 0.00
		TOTAL ADDITIONAL FEE:			$ 0.00

The Commissioner is hereby authorized to charge any additional fees required under 37 C.F.R. 1.16 or any patent application processing fees under 37 C.F.R. 1.17 associated with this communication, or credit any over payment to **Deposit Account No. 50-0687 under Order No. 20-143.**

Respectfully submitted,

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Date: February 27, 2007

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Atty Docket No.: **Balay 2-1**
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In re Patent Application of:
BALAY et al.
Title: **PCI/LVDS HALF BRIDGE**

February 27, 2007

(CORRECTED) APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Applicants submit herewith the following Appeal Brief as required by 37 C.F.R. § 41.37(c).

(1) REAL PARTY IN INTEREST

The real party in interest is Agere Systems Inc.

(2) RELATED APPEALS AND INTERFERENCES

The Applicants and their legal representatives and assignee are not aware of any other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the appending appeal.

(3) STATUS OF THE CLAIMS

Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 are pending in this application. Claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 stand rejected.

(4) STATUS OF AMENDMENTS

All amendments have been entered by the Examiner. No amendments were attempted subsequent to the Final Rejection issued by the Examiner on July 28, 2006.

(5) SUMMARY OF THE CLAIMED SUBJECT MATTER

Compact PCI (Peripheral Component Interconnect) has become a standard implementation for many telecommunications systems. Compact PCI provides a well-standardized backplane structure. With PCI, different line cards or blades of a system are connected with a PCI bus structure. As with any bus structure, the number of line cards that can be connected on a single PCI bus is limited. Typically five line cards are supported on a 33MHz PCI bus structure. For larger systems, multiple independent PCI segments have to be implemented, each supporting a limited number of elements.

The invention provides a system and method of overcoming the limitations associated with the number of line cards that can be connected to on a single bus through use of half bridge circuits connecting the bus segments. In particular, depending on the particular application, e.g., latency considerations, the data paths connecting the half bridge circuits are scalable to rely on more or less signal lines as needed for a particular application.

Claim 1 recites a system for interconnecting two or more computer bus architectures, e.g., elements 4 to 6 as shown in Fig. 1 with corresponding description on page 5, lines 7-15. It includes a first bus segment to transmit data information (3), a first half bridge circuit (4) to connect the first bus segment (3), a second bus segment (7) to transmit data information, a second half bridge circuit (6) to connect the first half bridge circuit (4), and to transfer data information between the first bus segment (3) and the second bus segment (7); and a

plurality of data paths (5) to connect the first half bridge circuit (4) and the second half bridge circuit (6). Importantly, claim 1 requires that the plurality of data paths (5) to connect the first half bridge circuit (4) and the second half bridge circuit (6) are **scalable to correspond to a bandwidth needed for a particular application**.

Referring to Fig. 1, claim 10 recites a method of interconnecting two or more computer bus architectures (3, 7) comprising connecting a first half bridge circuit (4) to a first bus segment (3). A second half bridge circuit (6) is connected to a second bus segment (7). The first bus segment (3) is connected to the second bus segment (7) through a plurality of data paths (5) connecting the first half bridge (4) and the second half bridge (6). Data information is transmitted from the first bus segment (3) to the second bus segment (7) over at least one of the plurality of data paths (5). Importantly, the plurality of data paths (5) connecting the first half bridge circuit (4) and the second half bridge circuit (6) are **scalable to correspond to a bandwidth needed for a particular application**.

Claim 19 recites, with reference to Fig. 1, a system for interconnecting two or more computer bus architectures (3, 7) comprising a first half bridge circuit means (4) connected to a first bus segment means (3). A second half bridge circuit means (6) is connected to a second bus segment means (7). A plurality of data paths means (5) connect the first half bridge circuit means (4) and the second half bridge circuit means (6). Wherein information is passed between the first bus segment means (3) and the second bus segment means (7) over the first half bridge circuit means (4) and said second half bridge circuit means (6). Importantly, the plurality of data paths means (5) are **scalable to correspond to a bandwidth needed for a particular application**.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) Whether claims 1-3, 6-8, 10-12, 15-17, 19-21 and 24-26 are obvious under 35 U.S.C. §103(a) over U.S. Patent No. 6,662,254 to Tal et al. (hereinafter "Tal") in view of *Lucent Technologies delivers new field-*

programmable system chips for high speed PCI bus and backplane data interfaces, press release November 08, 1999, cited as Relevant art in form PTO-892 as part of Paper No. 5, (hereinafter "Lucent").

(B) Whether claims 5, 14 and 23 are obvious under 35 U.S.C. §103(a) over Tal in view of U.S. Patent No. 6,457,091 to Lange et al. ("Lange").

(C) Whether claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25 and 26 are obvious under 35 U.S.C. §103(a) over U.S. Patent No. 6,457,091 to Lange et al. ("Lange") in view of Lucent.

(D) Whether claims 6, 15 and 24 are obvious under 35 U.S.C. §103(a) over Lange in view of Official Notice.

(7) ARGUMENT

(A) Claims 1-3, 6-8, 10-12, 15-17, 19-21 and 24-26 are not obvious under 35 U.S.C. § 103(a) over Tal in view of Lucent.

All claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 recite a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment. Moreover, claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 recite a plurality of **scalable** data paths connecting the half bridge circuits, scalable dependent upon a bandwidth needed for a particular application.

The Examiner acknowledged that Tal fails to disclose "that the serial channel comprising 4 full duplex pair can be 'scalable' depending on a bandwidth needed for a particular application (See Final Office Action dated July 28, 2006, page 5). However, the Examiner alleged that "Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing 'a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page 1, 4th paragraph, for providing design flexibility, functionality, and performance." (see Final Office Action dated July 28, 2006, page 5). The Examiner alleged that the "ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed and the fact that the ORT4622 half bridge contains a 4-

channel 622 megabit-per-second (2.5 gbps when all 4 channels are used clearly indicates that less then 4 channels can be ued when less bandwidth is needed)" (see Final Office Action dated July 28, 2006, page 5).

The Examiner relied on Lucent to allegedly disclose scalability. However, Lucent discloses that "Designers can use the device to drive high-speed data transfer across a backplane within a system" (see 4th full paragraph). Thus, a reading of Lucent reveals that the manufacturer of the ORT4622 intended its use across a backplane within a system. Although Applicants also disclose use of the ORT4622, Applicants disclose a novel use of a feature of the ORT4622 that is not disclosed as being used by Lucent within a backplane. The Examiner has still failed to provide a reference that discloses or suggests the use of **scalable** half bridge circuits between two bus segments, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26.

Moreover, the motivation that the Examiner provided to modify Tal is to provide Tal "with design flexibility/scalability, functionality, and speed/performance" that the Examiner acknowledged is disclosed by Lucent (see Final Office Action dated July 28, 2006, pages 6 and 11). Thus, the Examiner is simply reiterating benefits from a marketing statement associated with the ORT4622 not providing motivation why one or ordinary skill would modify Tal.

Moreover, the Applicants pointed out that "Teachings of references can be combined only if there is some suggestion or incentive to do so." In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). Nothing within Tal nor Lucent suggests modifying Tal with **scalable** half-bridge circuits. Thus, any modification of Tal without some suggestion for such a modification is based on improper hindsight.

Moreover, as the Examiner points out Tal discloses reliance on 4 full duplex pairs, each providing 622 mbps of bandwidth at page 6, lines 18-27 (see Final Office Action dated July 28, 2006, page 4). Thus, Tal teaches away from modification to use a scalable interface because it specifically requires use

of all four full duplex pairs for his application to provide "a bandwidth that will not hinder the eight slot per segment cPCI bus" (see col. 6, lines 18-19).

Thus, Tal in view of Lucent still fails to disclose or suggest a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of data paths connecting the half bridge circuits being scalable depending on a bandwidth needed for a particular application, as recited by claims 1-3, 6-8, 10-12, 15-17, 19-21 and 24-26.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Tal in view of Lucent does not render obvious any of claims 1-3, 6-8, 10-12, 15-17, 19-21 and 24-26. Thus, the rejection of claims 1-3, 6-8, 10-12, 15-17, 19-21 and 24-26 under 35 U.S.C. § 103(a) is improper and should be reversed.

(B) Claims 5, 14 and 23 are not obvious under 35 U.S.C. §103(a) over Tal in view of Lange.

All rejected claims 5, 14 and 23 recite a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment. Moreover, claims 5, 14 and 23 recite a plurality of **scalable** data paths connecting the half bridge circuits, scalable dependent upon a bandwidth needed for a particular application.

As discussed above, Tal fails to disclose or suggest a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of data paths connecting the half bridge circuits being scalable depending on a bandwidth needed for a particular application, as recited by claims 5, 14 and 23.

The Examiner relied on Lange to allegedly disclose a bridge that can have a bus width of either 32 bits or 64 bits (see Office Action dated July 28, 2006, page 7). However, a reading of Lange reveals that the bridge the Examiner refers to is "used to decouple a processor and an expansion bus" (see Lange col. 3, lines 58-61). Thus, Lange "scalability" lacks any real relevance to Applicants' claimed features, i.e., Lange, like Tal, fails to disclose **scalable** half

bridge circuits connecting a first bus segment and a second bus segment, as recited by claims 5, 14 and 23.

Thus, Tal modified by Lange would at best theoretically result in Tal using a bus width of 32 bits or 64 bits "to decouple a processor and an expansion bus". Tal modified by Lange would still fail to disclose or suggest a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of **scalable** data paths connecting the half bridge circuits, scalable dependent upon a bandwidth needed for a particular application, as recited by claims 5, 14 and 23.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Tal in view of Lange does not render obvious any of claims 5, 14 and 23. Thus, the rejection of claims 5, 14 and 23 under 35 U.S.C. § 103(a) is improper and should be reversed.

(C) Claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25 and 26 are not obvious under 35 U.S.C. § 103(a) over Lange in view of Lucent Technologies.

All rejected claims 1-3, 6, 8, 10-12, 15, 17, 19-21, 24 and 26 recite a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of **scalable** data paths connecting the half bridge circuits, scalable dependent upon a bandwidth needed for a particular application.

The Examiner acknowledged that Lange fails to disclose "that the serial channel comprising 4 full duplex pair can be 'scalable' depending on a bandwidth needed for a particular application (See Final Office Action dated July 28, 2006, page 9). However, the Examiner alleged that "Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing 'a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page 1, 4th paragraph, for providing design flexibility, functionality,

and performance." (see Final Office Action dated July 28, 2006, page 9). The Examiner alleged that the "ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed and the fact that the ORT4622 half bridge contains a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used clearly indicates that less then 4 channels can be sued when less bandwidth is needed" (see Final Office Action dated July 28, 2006, page 9).

The Examiner relied on Lucent to allegedly disclose scalability. However, as discussed above, Lucent discloses that "Designers can use the device to drive high-speed data transfer across a backplane within a system" (see 4th full paragraph). Thus, a reading of Lucent reveals that the manufacturer of the ORT4622 intended its use across a backplane within a system. Although Applicants also disclose use of the ORT4622, the Applicants disclose a novel use of a feature of the ORT4622 that is not disclosed as being used by Lucent within a backplane. The Examiner has still failed to provide a reference that discloses or suggests the use of scalable half bridge circuits between two bus segments, as recited by claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25 and 26.

Moreover, the motivation that the Examiner provides to modify Lange is to provide Lange "with design flexibility/scalability, functionality, and speed/performance" that the Examiner acknowledged is disclosed by Lucent (see Final Office Action dated July 28, 2006, page 11). Thus, the Examiner is simply reiterating benefits from a marketing statement associated with the ORT4622 not providing motivation why one or ordinary skill would modify Lange.

Moreover, the Applicants pointed out that "Teachings of references can be combined only if there is some suggestion or incentive to do so." In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). Nothing within Lange nor Lucent suggests modifying Lange with scalable half-bridge circuits. Thus, any modification of Lange without some suggestion for such a modification is based on improper hindsight.

Moreover, Lange discloses use of a single serial communication line (see Fig. 4, item 131). Thus, Lange teaches away from the Examiner's alleged modification of use of more than one data line that would add cost and complexity to his system because requiring use of only one data line for his application.

Thus, Lang modified by Lucent would still fail to disclose or suggest a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of data paths connecting the half bridge circuits being scalable depending on a bandwidth needed for a particular application, as recited by claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25 and 26.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Lange in view of Lucent does not render obvious any of claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25 and 26. Thus, the rejection of claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25 and 26 under 35 U.S.C. § 103(a) is improper and should be reversed.

(D) Claims 6, 15 and 24 are not obvious under 35 U.S.C. § 103(a) over Lange in view of Official Notice.

All rejected claims 6, 15 and 24 recite a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of **scalable** data paths connecting the half bridge circuits, scalable dependent upon a bandwidth needed for a particular application.

As discussed above, Lange fails to disclose or suggest a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of scalable data paths connecting the half bridge circuits being scalable depending on a bandwidth needed for a particular application, as recited by claims 6, 15 and 24.

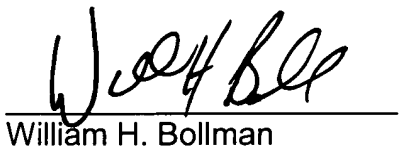
Official Notice was relied on to disclose two PCI buses having substantially same frequencies. Thus, Lange even in view of two PCI buses having substantially same frequencies still fails to disclose or suggest **scalable** signal lines between two half bridge circuits, i.e., Lange even in view of the unsupported Official Notice fails to disclose or suggest a method and apparatus relying on a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of **scalable** data paths connecting the half bridge circuits, scalable dependent upon a bandwidth needed for a particular application, as recited by claims 6, 15 and 24.

It is respectfully submitted that not only does this rejection fail on its face, and thus is improper, but also in light of the above comments its clear that Lange in view of Official Notice does not render obvious any of claims 6, 15 and 24. Thus, the rejection of claims 6, 15 and 24 under 35 U.S.C. § 103(a) is improper and should be reversed.

CONCLUSION

For all the reasons set forth above, the rejections of claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26 are improper and should be reversed. The Applicants therefore respectfully request that this Appeal be granted and that the rejections of the claims be reversed.

Respectfully submitted,



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CLAIMS APPENDIX

CLAIMS INVOLVED IN THE APPEAL

1. A system for interconnecting two or more computer bus architectures, comprising:

a first bus segment to transmit data information;

a first half bridge circuit to connect said first bus segment;

a second bus segment to transmit data information;

a second half bridge circuit to connect said first half bridge circuit, said second half bridge circuit to transfer data information between said first bus segment and said second bus segment;

a plurality of data paths to connect said first half bridge circuit and said second half bridge circuit;

wherein said plurality of data paths to connect said first half bridge circuit and said second half bridge circuit are scalable to correspond to a bandwidth needed for a particular application.

2. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment is a PCI architecture bus.

3. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said second bus segment is a PCI architecture bus.

4. (canceled)

5. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment operates at a different bus frequency than a bus frequency of said second bus segment.

6. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment operates at a substantially same bus frequency as a bus frequency of said second bus segment.

7. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

at least one of said first half bridge circuit and said second half bridge circuit are field programmable.

8. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

9. (canceled)

10. A method of interconnecting two or more computer bus architectures comprising:

connecting a first half bridge circuit to a first bus segment;

connecting a second half bridge circuit to a second bus segment;

connecting said first bus segment to said second bus segment through a plurality of data paths connecting said first half bridge and said second half bridge; and

transmitting data information from said first bus segment to said second bus segment over at least one of said plurality of data paths;

wherein said plurality of data paths to connect said first half bridge circuit and said second half bridge circuit are scalable to correspond to a bandwidth needed for a particular application.

11. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

said step of transmitting data transmits data over a SCSI architecture bus.

12. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

said step of transmitting data transmits data over a PCI architecture bus.

13. (canceled)

14. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

operation of a bus frequency of said first bus segment is different than a bus frequency of said second bus segment.

15. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

operation of a bus frequency of said first bus segment is substantially the same as a bus frequency of said second bus segment.

16. A method for interconnecting two or more computer bus architectures according to claim 10, further comprising:

field programming at least one of said first half bridge circuit and said second half bridge circuit.

17. A method for interconnecting two or more computer bus architectures according to claim 10, further comprising:

recovering a clock signal for said first half bridge circuit and said second half bridge circuit from their respectively connected said first bus segment and said second bus segment.

18. (canceled)

19. A system for interconnecting two or more computer bus architectures comprising:

a first half bridge circuit means connected to a first bus segment means;

a second half bridge circuit means connected to a second bus segment means; and

a plurality of data paths means to connect said first half bridge circuit means and said second half bridge circuit means;

wherein information is passed between said first bus segment means and said second bus segment means over said first half bridge circuit means and said second half bridge circuit means; and

wherein said said plurality of data paths means are scalable to correspond to a bandwidth needed for a particular application.

20. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment is a PCI architecture bus.

21. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said second bus segment means is a PCI architecture bus.

22. (canceled)

23. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment means bus frequency is different than said second bus segment means bus frequency.

24. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment means bus frequency is the same as said second bus segment means bus frequency.

25. The system for interconnecting two or more computer bus architectures according to claim 19, further comprising:

at least one of said first half bridge circuit means and said second half bridge circuit means are field programmable.

26. The system for interconnecting two or more computer bus architectures according to claim 19, further comprising:

said first half bridge circuit means and said second half bridge circuit means recover a clock signal from their respectively connected said first bus segment means and said second bus segment means.

27. (canceled)

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None